Mid-term Examination - Semiconductor devices II – Spring 2022 (Ionescu)

Select by a CIRCLE, ONE or MORE correct answers for each of the questions below.

Each good answer is marked by +1, each wrong answer is marked by -1

Even if not mandatory, you can motivate your answer under 'Comments'.

Question 1: *CMOS Technology Boosters*

The nanometer CMOS performance enabled by so called technology boosters (by definition, a technology innovation that improves some of the device performance in static and/or dynamic operation) are applied, such as strain, high-k dielectrics, metal gate, new channel replacement materials, etc.

Select the correct statements concerning such performance boosters.

1. The **subthreshold swing** of an n-type MOSFET can be improved by the changing the material channel, for instance replacing silicon with a III-V material like InAs.
2. **Tensile strain** improves the mobility of and holes in p-type MOSFETs, and, therefore, is a performance booster of these types of devices.
3. The use of a **high-k dielectric** to achieve the same gate capacitance instead of using SiO2 as dielectric reduces the gate leakage current.
4. **SiGe (silicon-germanium) or Germanium materials** can be used in combination with a silicon channel to generate local material stress.
5. **A junctionless transistor** has the source, channel and drain doping of same type (n OR p).
6. The **Ioff current** is typically higher in Germanium MOSFETs compared to Silicon MOSFETs, at similar transistor dimensions and voltage biases.
7. A **very thin channel resulting in a Fully Depleted (FD) SOI MOSFET used as technology booster** reduces the leakage of source and drain junctions.
8. The **Gate-All-Around (GAA) transistor** is not a multi-gate transistor.
9. High-k dielectrics and multigate transistor architecture are **additive technology boosters,** which means that they can be simultaneously applied to a MOSFET to improve its performance.
10. Using a **silicon nanowire** instead of a bulk silicon channel in a gate-all-around nanowire FET is a technology booster.

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Comments on Question 1:

Question 2: MIT switches

The Metal-Insulator-Transition (MIT) switch can be considered as a steep slope switch exploiting the phase change in some functional oxides.

Choose the correct properties of MIT switches from the below statements.

1. The **mechanism of switching** the current in a MIT switch corresponds to a change of the equivalent bandgap of the MIT material.
2. The **mechanism of switching** the current in a MIT switch structural change of the atom positions in the MIT material.
3. In a three terminal MIT switch with an insulating gate control over a VO2 material substrate, the **ON state under positive gate voltage corresponds to the formation of an inversion layer of electrons** created at the surface of the MIT switch, induced at the transition temperature.
4. The **switching mechanism in VO2 two-terminal switch** from OFF to ON state turns a CAPACITOR to a RESISTOR, from an electrically equivalent circuit point of view, which mean this mechanism can be potentially used to reconfigure the characteristics of Radio Frequency Filter.
5. The **bandgap of the VO_2 switch** in the OFF state (insulating) dictates its ION current.
6. The **MIT and IMT transition temperatures** of VO2 can be modulated by doping with metals.
7. **The carrier mobility in VO2 material** below the transition temperature dictates the level of ON current.
8. The VO_2 switch has a subthermionic abrupt swing between OFF and ON states that has a very little dependence on temperature.
9. The switching mechanism in VO_2 switches is non-hysteretic.
10. A VO2 switch has **transition times (OFF to ON and ON to OFF)** typically larger that micrometer site MEMS switches.
11. The thin VO_2 layer can be used as an **optically tunable metamaterial coating** (a material with electrically controlled optical properties such as reflection), in infrared and far-infrared wavelengths.

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Comments on Question 2:

Question 3: Comparison of MEMS, Negative Capacitance Switches and SOI MOSFET logic switches.

A. Enumerate five (5) advantages of MEMS switch compared to a Negative Capacitance MOSFET
B. Enumerate five (5) advantages of a Tunnel FET compared to a Negative Capacitance FETs.
C. Enumerate five (5) advantages of a fully depleted SOI MOSFET versus a partially-depleted SOI MOSFET.

A)

1)

2)

3)

4)

5)

B)

1)

2)

3)

4)

5)

C)

1)

2)

3)

4)

5)

Question 4: Tunnel FETs

The Tunnel FET is a gated p-i-n diode device operating in reversed bias regime and exploiting quantum-mechanical band-to-band tunneling. Select the correct properties of this steep slope device:

Choose the correct properties of Tunnel FET switches from the below statements.

1. A **Tunnel FET with Germanium source** and a silicon Channel, having the same geometry and dimensions as an all-silicon Tunnel FET has a lower Ion current.
2. A **Tunnel FET with Germanium source** and a silicon Channel, having the same geometry and dimensions as an all-silicon Tunnel FET has a lower Ioff current.
3. **Trap-Assisted Tunneling (TAT)** is a phenomenon that does not depends on temperature but only on the energy levels of traps.
4. The **temperature dependence** trend of subthreshold characteristics of Tunnel FET is very similar to the one of MOSFETs made of same semiconductor material; the subthreshold slope degrades with the temperature increase.
5. **Carrier mobility** plays a key role in the transport characteristics of Tunnel FETs. Thus, materials with higher carrier mobility like III-V and Ge are suitable for these devices.

6. The **leakage current, Ioff, of Tunnel FETs** at cryogenic (sub-77K) temperatures is higher than at room temperature.
7. The **Electron-Hole Bilayer Tunnel FET** is a Density of States switch that can achieve a steeper transition between off and on than a conventional Tunnel FET because the gate-controlled electrostatic field and the tunneling paths are aligned.
8. Tunnel FET exploits a **discrete charge conduction principle** (electrons tunnel one by one from the conduction to the valence band).
9. The **steep-slope of Tunnel FETs** is normally steeper at lower levels of currents.
10. The output characteristics of Tunnel FETs saturate by carrier velocity saturation, as in case of nanometer scale MOSFETs.
